REMARKS

In the Office Action, Claims 8, 9, 12-15, 17, 19-21 and 30-32 are pending and stand rejected. In this response, Claims 8, 15, 19, and 30 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 8, 9, 12-15, 17, 19-21 and 30-32 in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 8-9, 12-14 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,477,623 ("Jeddeloh") in view of U.S. Patent No. 6,625,673 issued to Dickey ("Dickey").

Regarding Claim 8, Claim 8 recites the following claim feature, which is neither taught nor suggested by the combination of Jeddeloh in view of Dickey:

> 8. A method, comprising:
> populating entries within a conversion table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory, wherein the physical addresses have a greater number of bits than the virtual addresses to enable paging to off-chip components for access to the main memory above a physical address range limit imposed by a register/bus width;
> using the conversion table to translate a virtual address from the graphics controller to a first physical address for access to the main memory; and
> using the conversion table to translate a virtual address from a bus controller to a second physical address for access to the main memory;
> wherein the second physical address has a greater number of bits than the virtual address from the graphics controller and the second physical address has a greater number of bits than the virtual address from the bus controller. (Emphasis added.)

As correctly noted by the Examiner, Jeddeloh does not disclose the second address having a greater number of bits than the first address and the fourth address having a greater number of bits than the third address, as recited by Claim 8. As a result, the Examiner cites Dickey.

Regarding Dickey, Dickey is devoid of any teachings or suggestions with regards to providing physical address translation and paging to off-chip components, such as, for example, graphics controllers and I/O devices for access to memory above the 4 GB limit imposed by 32-bit bus and register widths. According to the Examiner, Jeddeloh does not explicitly suggest expanding the address space for I/O devices. (*See* page 3 of the Office Action mailed 01/17/2007.) According to the Examiner:

> Dickey teaches mapping a first address to a second address, wherein the second address has a greater number of bits than the first address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). (*See* page 3, paragraph 1 of the Office Action mailed 07/27/2007.)

Based on the cited passage above, Applicants respectfully submit that the Examiner has incorrectly equated I/O address mapping techniques, as taught by Dickey, with the translation of addresses received from graphics controllers and I/O devices (off-chip devices) into a translated address for access to memory based on, for example, a previously assigned portion of memory using a memory allocation command (e.g., malloc). We submit that off-chip devices do not share a processor's view of main memory because they do not have access to the processors paging tables. In other words, as known to those skilled in the art, memory mapped I/O, as taught by Dickey, provides an address assignment mechanism for the various bridges and I/O devices in a computer system. This technique assigns a portion of the processor address space to the various I/O device to enable access such I/O devices.

For example, to access an I/O device, the processor issues a transaction to a memory address which is detected by, for example, a memory controller or other like device, as mapped to an I/O device. In response to such detection, the memory controller or in the case of Dickey, the host bridge identifies that the memory address is mapped to a respective I/O device and directs the transaction to the respective I/O device.

Accordingly, Dickey teaches that:

> Host I/O bridge m . . . translates the (n+l)-bit processor view I/O address to a 32-bit I/O device view I/O address. (Col. 5, lines 1-5).

Hence, the I/O address mapping technique taught by Dickey:

> Provides a pre-assigned address region, which is guaranteed to be available, to each of the I/O device in the system, and thus provide the convenience on-line replacement of various I/O devices having different memory capacity requirements without causing an out-of-address-space problem associated with fragmentation of I/O memory space in the system memory. (Col. 6, lines 17-23) (Emphasis added.)

Therefore, as illustrated in reference to FIG. 4 of Dickey, the teachings of Dickey are expressly limited to the translation of a processor view address 401 which may be 40 bits into an I/O device view address 403 which is comprised of 32 bits. As described by Dickey:

> The I/O mapping utilizes a greater number of address bits than the address bits available from I/O devices to assign a much larger address space to each device by translating the larger number of bits address from the system to the smaller number of bits address of the I/O devices. (Col. 3, lines 61-66) (Emphasis added.)

However, Applicants respectfully submit that such I/O devices are still limited to access within the 4 GB range as provided by 32-bit addresses. Hence, although Dickey expands the I/O address space for the various bridges and peripheral devices connected to a computer system as taught by Dickey, this expansion is simply limited to the processor's view to conveniently provide the processor with additional addresses for assignment to the various I/O devices and does not provide the similar capability to such I/O devices; namely, such I/O devices remain prohibited from access to memory above the 4 GB limit imposed by 32-bit I/O device bus and register widths.

Hence, the teachings of Jeddeloh in view of Dickey would not suggest modification of the address translation using the GART table of Jeddeloh to extend the physical address space for access to memory, as in Claim 8, since the teachings of Jeddeloh are specifically limited to addressing the following problem described in the Background of Jeddeloh:

> Data transfers between processor and graphics controller, and between graphics controller and system memory are presently constrained by the bandwidth of the busses and their data channels that couple these components together. (col. 1, lines 56-60.) (Emphasis added.)

As specifically indicated in the Background of Jeddeloh, what is needed is a computer system architecture that facilitates high-bandwidth data transfers between a graphics controller and other system components. (*See*, col. 2, lines 11-13.) To achieve this goal, Jeddeloh teaches data paths, which connect the graphics controller and other devices to switch 124 (FIG. 2) to have a greater width than the busses typically couple computer system components together.

In other words, the teachings of Jeddeloh are directed to providing high-bandwidth communications and not directed to physical address range limitations caused by bus and register widths for accessing memory above the 4GB limit imposed by 32-bit bus and register widths. Furthermore, the teaching of Dickey are limited to preventing I/O fragmentation and also not directed to providing I/O device with access to memory above the 4 GB limit.

Therefore, we conclude that an artesian having common sense at the time of the invention, would not have reasonably considered modification of the address translation using the GART table of Jeddeloh in view of Dickey in the manner suggested by the Examiner to extend the physical address space for access to memory since neither the teachings of Jeddeloh, which are directed to providing high bandwidth communications nor the teachings of Dickey, which are limited to providing I/O fragmentation, are directed to providing address translation and paging for off-chip devices to access to memory above a physical address range limit imposed by a register/bus width, as in Claim 8.

Hence, no combination of Jeddeloh in view of Dickey could teach or suggest populating entries within a conversion table to map virtual address of a memory range allocated to a graphics controller to physical address with main memory, wherein the physical addresses have a greater number of bits than the virtual addresses to enable paging to off-chip components for access to the main memory above a physical address range limit imposed by a register/bus width, as in Claim 8.

For each of the above reasons, therefore, Claim 8, and all claims which depend from Claim 8, are patentable over the cited art.

Each of Applicant's other independent claims include features similar to those highlighted above, with reference to Claim 8. Therefore, all of Applicant's other independent

claims, and all claims which depend from them, are also patentable over the cited art, for similar reasons.

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is submitted that the pending claims patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 9/24/07
Elaine Kwak Date